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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHEW, JOHN	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 07/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,832	MITTAL ET AL.	
	Examiner	Art Unit	
	John L Shew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-26,28-31,33-34,36-43,45-47 is/are rejected.

7)☒ Claim(s) 27,32,35 and 44 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 05/07/01 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because

FIG. 2 reference character 44 identifies item as "TRAFFIC MANAGER CONTROLLER", disclosure page 7 line 17 identifies item as "MEMORY HUB CONTROLLER".

FIG. 2 "INGRESS FLOW ID #1" should be "INGRESS QUEUE #1".

FIG. 7 reference character 132 identifies item as "INGRESS MEMORY HUB", disclosure page 17 line 13 identifies item as "EGRESS MEMORY HUB".

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement

sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

Page 13 line 25 cites "packet C" should be "packet B".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-18, 20-26, 28, 30-31, 33-34, 36-43 and 45-47 are rejected under 35 U.S.C. 102(b) as being anticipated by Merchant et al.

Claim 1, Merchant teaches a memory hub (FIG. 1, column 2 lines 65-67, column 3 lines 1-15) referenced by Integrated Multiport Switch 12a which uses memory and functions as a hub to a plurality of stations 14, comprising a first ingress interface for receiving from a source port packets having associated ingress flows (FIG. 3A, column 6 lines 9-15) referenced by MAC Port 1 70a of receiving portion 20a, a second ingress interface for outputting packets or cells to a switch fabric (FIG. 3A, column 6 lines 32-35) referenced by Queuing Logic 74 of MAC Port 1 70a outputs to switching fabric of Port Vector FIFO 56, and an ingress controller that queues the packets or cells according to the associated ingress flows (FIG. 3A, column 6 lines 32-35, lines 40-42) referenced by Queuing Logic 74 transfer of data from internal receive FIFO queue to external memory interface controller 44.

Claims 2-5, Merchant teaches an ingress traffic manager that schedules how the packets or cells are output to the switch fabric (FIG. 3A, column 6 lines 46-50) referenced by Scheduler 80 controlling memory access by queuing logic 74. Merchant teaches the ingress traffic manager schedules outputting of the packets on a per flow basis or Class of Service basis per destination basis (column 5 lines 30-38) referenced by IRC 40 output of a forwarding descriptor including priority, port vector, VLAN, opcode and frame pointer wherein priority is the flow basis, Class of Service is associated to a VLAN and destination is associated to a port vector. Merchant teaches the ingress controller (FIG. 3A) referenced by Queuing Logic 74, manages memory operations for

queuing the packets or cells (column 6 lines 32-35, lines 40-42) referenced by transfer of data from internal receive FIFO queue to external memory interface controller 44, independently of controls from the ingress traffic manager (FIG. 3A, FIG. 3B, column 5 lines 5-14) referenced by IRC 40 which monitors the data bus to determine header information along with separate units for Queuing Logic 74 and IRC 40. Merchant teaches the ingress controller and the ingress traffic manager are separate circuits operating on separate integrated circuits (FIG. 3A, FIG 3B) referenced by Queuing Logic as a separate unit from Internal Rules Checker 40.

Claim 6, Merchant teaches a Class of Service Queuer that receives packets or cells output from the second ingress interface on a per flow basis (FIG. 3A, FIG 3B) referenced by Internal Rules Checker 40 monitoring each Queuing Logic 74 output which is on a per flow basis based on source port, and sends the packets or cells to the switch fabric on a per Class of Service associated basis (column 5 lines 30-38, column 10 lines 41-52) referenced by IRC 40 output of a forwarding descriptor including priority, port vector, VLAN, opcode and frame pointer used for routing, Class of Service is associated to a VLAN.

Claim 8, Merchant teaches ingress queues maintaining pointers to the queued packets or cells according to ingress flows (FIG. 3A, column 4 lines 61-67, column 5 lines 1-4) referenced by the use of frame pointers to map the outputs of the received FIFO queues

of the Queuing Logic 74 which are the ingress flows to the external memory interface 44.

Claim 9, Merchant teaches egress flow fields for assigning egress flow Ids to the packets or cells according to the associated ingress flows (column 5 lines 30-48) referenced by the forwarding descriptor's frame pointer which is representative of egress flow fields, use of frame pointer to select appropriate output queues which is representative of egress flow Ids and receive port number which is associated to ingress flows.

Claims 10 and11, Merchant teaches forwarding label fields for assigning forwarding labels to the packets or cells (column 5 lines 30-48) referenced by forwarding descriptor's port vector identifying destination ports, according to the associated ingress flows (column 5 lines 30-48) referenced by receive port number. Merchant teaches the forwarding labels contain information for establishing a path in the switching fabric to a destination port (column 5 lines 30-48) referenced by forwarding descriptor's port vector identifying destination ports where the packet is routed.

Claim 12, Merchant teaches a Class of Service fields for assigning Class of Service values to the packets or cells (column 5 lines 30-48, column 10 lines 44-52) referenced by the VLAN information and VLAN vector of ports wherein each VLAN represents a Class of Service corresponding to different port speeds.

Claims 13-18, Merchant teaches an egress controller having a first interface (FIG. 3A) referenced by Output Queue Write Side Mgmt Port 68a, for receiving packets or cells output from the switch fabric (FIG. 3A) referenced by Port Vector FIFO 56, having associated egress flows (FIG. 4, column 8 lines 58-65) referenced by flows based on Egress Rules 112, a second interface for transferring the packets to a destination port (FIG. 3A) referenced by Dequeuing Logic 76, and an egress controller configured to manage how the packets are queued to the destination port according to the associated egress flows (FIG. 3A, column 5 lines 42-56) referenced by the management queue 68 receiving a frame pointer for processing by a management agent followed by the the output queue 58 supplying the frame pointer to the dequeuing block 76 for fetching the data. Merchant teaches egress queues for maintaining pointers to the packets or cells received from the switch fabric according the associated egress flows (FIG. 3A, FIG. 3B, column 5 lines 42-56) referenced by Output Queues 68 receiving frame pointers for data management. Merchant teaches forwarding label fields for identifying forwarding labels for egress queues (column 5 lines 30-48) referenced by forwarding descriptor's port vector identifying destination MAC ports which associates the required egress queue. Merchant teaches the forwarding label fields identify source ports (column 5 lines 30-48) referenced by forwarding descriptor's receive port number.

Merchant teaches content addressable memory (FIG. 4) referenced by MAC Address Table 114, that maps the egress flows (column 5 lines 30-38) referenced by frame pointers, to the egress queues (FIG. 3A) referenced by Output Queues 68. Merchant

teaches an egress traffic manager (FIG. 4, column 2 lines 53-54) referenced by Internal Rules Checker, that receives egress flow information from the egress controller and schedules the egress controller to output packets to the destination port according to the egress flow information (FIG. 4, column 7 lines 21-29) referenced by reception of frame pointer and determination of output queue for the destination port scheduled by IRC Scheduler 104.

Claim 20, Merchant teaches a method for forwarding packets in a network processing device (Abstract lines 1-3) referenced by data forwarding in a network switch, comprising receiving packets associated with ingress flows (FIG. 3A, column 6 lines 9-15) referenced by the receive portion 20a, queuing the packets associated with the ingress flows (FIG 3A) referenced by Queuing Logic 74 associated to the MAC Ports of the ingress flows, identifying ingress flow information for the packets (column 5 lines 5-21) referenced by the IRC snoop of data for source address information, and outputting the queued packets according to the ingress flow information (column 4 lines 61-67, column 5 lines 1-4 lines 30-32) referenced by output to an external memory based on frame pointer from ingress information.

Claims 21-26, 28, 30-31, 33-34 and 36-37, Merchant teaches managing memory operations for queuing the packets in a first integrated circuit (FIG. 3A) referenced by Queuing Logic unit 74, and independently managing in a second integrated circuit how the queued packets are scheduled for being output (FIG. 3A) referenced by Scheduler

unit 80 which is separate from unit 74. Merchant teaches outputting the packets on a per flow basis or on a per Class of Service basis (column 5 lines 30-38) referenced by IRC 40 output of a forwarding descriptor including priority, port vector, VLAN, opcode and frame pointer wherein priority is the flow basis and Class of Service is associated to a VLAN. Merchant teaches outputting the packets on a per flow basis (FIG. 3A) referenced by the Output Queues 58a with priority 0 and priority 1, and requeuing the output packets for outputting to a switch fabric on a per Class of Service basis (FIG. 4, column 10 lines 42-52) referenced by subsequent routing based on VLAN assignment. Merchant teaches identifying egress flows (FIG. 3A) referenced by Output Queues 68, for the ingress flows (FIG. 3A) referenced by MAC Ports 70 with associated Queuing Logic, and assigning the identified egress flows to the packets before being output (column 5 lines 30-48) referenced by forwarding descriptor's port vector identifying destination MAC ports which associates the required egress queue. Merchant teaches identifying forwarding labels for ingress flows (column 5 lines 30-48) referenced by port vector for forwarding labels and receive port number for ingress flows, and assigning the identified forwarding labels to the packets before being output (column 5 lines 30-32) referenced by output of forwarding descriptor to switch subsystem prior to output of data packet. Merchant teaches identifying a Class of Service for the ingress flows and assigning the Class of Service to the packets before being output to the switch fabric (column 5 lines 30-48) referenced by forwarding descriptor's VLAN information as a Class of Service and a receive port number for the ingress flow. The forwarding descriptor is sent to the switch subsystem prior to output of the associated data packet.

Merchant teaches tracking ingress flow information for the packets (column 5 lines 30-32) referenced by forwarding descriptor's receive port number, and scheduling the packets for outputting to a switch fabric according to the tracked ingress flow information (FIG. 3A, column 6 lines 46-62, column 7 lines 8-23) referenced by Scheduler 80 to output to the external memory in association with the forwarding descriptor for routing through the switch subsystem. Merchant teaches receiving the packets with associated egress flows from a switch fabric (FIG. 3A, FIG. 3B, column 5 lines 42-46) referenced by Port Vector FIFO 56 as the switch fabric decoding the forwarding descriptor including port vector, and queuing the packets for outputting to destination ports according to the egress flows (FIG. 3A) referenced by Output Queues 68 associated to Dequeuing Logic 76 and MAC port wherein the the port vector is used to determine the Output Queue. Merchant teaches associating forwarding labels (column 5 lines 42-46) referenced by port vector, and ingress flows (FIG. 3A) referenced by input MAC Port 70a with Queuing Logic, with egress flows for the packets received from the switch fabric (FIG. 3A, column 5 lines 42-46) referenced by Output Queue 68 based on forwarding descriptor. Merchant teaches identifying unused egress queues for each egress port associated with a multicast packet (FIG. 3C, column 7 lines 59-67, column 8 lines 5) referenced by frame pointers from free buffer queue and multicopy transmission wherein port vector designates multiple ports, using a common CAM value to map to the unused egress queues in each egress port (FIG. 4, column 11 lines 50-53) referenced by Multicast Flood Vectors table 118 to route to appropriate VLAN output queues, and assigning the CAM value to the multicast packet as an

egress flow value (column 11 lines 39-53) referenced by the determination of output ports which equate to egress flow value. Merchant teaches receiving a multicast packet from a switch fabric (FIG. 3B, column 11 lines 31-38) referenced by data forwarding from Port Vector FIFO to Output Queue based on VLAN associated to multicast frame, using the CAM value in the multicast packet to access a content addressable memory (FIG. 4, column 11 lines 31-38) referenced by VLAN as CAM value to lookup in Multicast Flood Vectors table 118, using an egress queue mapped by the content addressable memory as the egress queue for the multicast packet (FIG 3A) referenced by Output Queues 68 determined by Multicast Flood Vectors table 118. Merchant teaches providing an Egress flow Id (column 5 lines 30-38) referenced by port vector, Class of Service (column 5 lines 30-38) referenced by VLAN information, or forwarding label value with the received packets (column 5 lines 30-38) referenced by destination port identified by port vector. Merchant teaches providing an Egress flow Id, Class of Service or forwarding label value in a memory hub data structure (column 5 lines 30-42) referenced by output of forwarding descriptor with port vector, VLAN information and destination port to switching subsystem, which must be stored in memory for processing.

Claims 38-43 and 45-47, Merchant teaches a memory hub (FIG. 1) referenced by Integrated Multiport Switch 12a, comprising a first interface for receiving packets or packet fragments having associated flow Ids (FIG. 3A) referenced by Output Queue 68a receiving packets wherein flow Id is the receive port number, a second interface for

outputting the packets or packet fragments (FIG. 3A) referenced by Dequeue Logic 76 and MAC Port 1 70c which transmits the data packet, and a controller that queues the packets or packet fragments in a memory according to the associated flow Ids (column 5 lines 30-56) referenced by Output Queue Write Side Mgmt Port 68a which uses frame pointers associated to ports to fetch data from memory for management processing. Merchant teaches the controller receives control signals identifying the flow Ids for queuing the packets and receives control signals for identifying the flow Ids for dequeuing the packets (FIG. 3A) referenced by Output Queue Write Side Mgmt Port 68a receiving control signals for queuing of data packets and Dequeuing Logic 76 receiving control signals for dequeuing of data packets. Both controllers use frame pointers locate and transfer data packets to and from external memory. Merchant teaches the first interface receives the packets or packet fragments from a switch fabric (FIG. 3A, FIG. 3B) referenced by Output Queue 68 receiving data from the Port Vector FIFO 56, and the second interface outputs packets to an egress packet processor (FIG. 3A) referenced by Dequeuing Logic 76 which processes outputs to a MAC Port 70c for output transmission. Merchant teaches another memory hub having a first interface configured to receive packets from the egress packet processor and a second interface configured to output packets to an egress interface (FIG. 1) referenced by a number of Integrated Multiport Switches 12a 12b 12c networked together such that one IMS transmits data to and from another IMS. Merchant teaches traffic manager that receives packet lengths associated with the packets output from the egress packet processor (FIG. 3A, FIG. 5) referenced by MAC Port 70c which receives packets

including a Length field 2B from the Dequeuing Logic 76. Merchant teaches a traffic manager that receives packet lengths associated with the packets received from the first interface (FIG. 3A, FIG. 5) referenced by MAC Port 1 which receives packets from Output Queue 68 via Dequeuing Logic 76 which packet include a Length field 2B. Merchant teaches the packets or packet fragments include an egress flow Id, Class of Service or forwarding label value (FIG. 5, FIG. 6, column 9 lines 50-59) referenced by an IEEE 802.1Q packet with the addition of a VLAN header so the associated fields are destination Address 6B, VLAN Identifier and Source Address. Merchant teaches a data structure that includes an egress flow Id, Class of Service or forwarding label value (column 5 lines 30-42) referenced by output of forwarding descriptor with port vector for egress flow Id, VLAN information for Class of Service and destination port for forwarding label to the switching subsystem, which must be stored in memory for processing. Merchant teaches the controller sends packet length values to a traffic manager associated with the flow Ids (FIG. 3A, FIG. 5) referenced by Output Queue Write Side Mgmt Port sends the IEEE802.1Q packet including a Length field 2B to the Dequeuing Logic 76 associated to the output ports which are flow Ids.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 19 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merchant et al. as applied to claims 1-6, 8-18, 20-26, 28, 30-31, 33-34, 36-43 and 45-47 above, in view of Opalka et al.

Claims 7 and 29, Merchant teaches a forwarding scheme for a multiport network switch. Merchant does not teach a traffic manager directing the dropping of packets or cells that back up. Opalka teaches an ingress traffic manager that drops frames or cells (FIG. 14, column 14, lines 59-67, column 15 lines 1-4) referenced by an ingress forward engine that determines when frames or cells are dropped including queues of ingress flow that are full which is indicative of tracked ingress flow information. This function associates to the ingress traffic manager directing the ingress controller to drop packets.

Claim 19, Opalka teaches dropping packets or cells for egress queues that back up (column 20 lines 59-67, column 21 lines 1-11) referenced by the dropping of data for buffers of queues are filled on egress NeoN ports. This function associates to the egress traffic manager notifying the egress hub to drop packets.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate dropping the cell when it is determined the ingress or egress queues are full as suggested by the determination engine of Opalka to the multiport switch network of Merchant for the purpose of maintaining traffic operations in the network.

Allowable Subject Matter

5. Claims 27, 32, 35 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Citation of Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent 6574232, Honig discloses a crossbar switch utilizing broadcast buffers and associated management.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L. Shew whose telephone number is 703-305-8708. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 703-305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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